ABSTRACT

An output signal of a CCD or other solid-state
imaging device (101) is converted at an A/D converter
(102) into a digital signal, which is in turn loaded in a
5   latch (103). The latch (103) comprises a delay unit, a
line memory, etc. to hold pixel data demanded by a
defective pixel detection algorithm. A normal pixel
detection block (104) is adapted to receive a signal from
the A/D converter (102) to determine whether the pixel to
10   be inspected is a normal one or a possibly defective one,
and send out the result of determination to a defective
pixel detection block (105). When the pixel to be
inspected is determined as defective, a defective pixel
correction block (106) is operable to implement correction
15   processing, producing a correction output (107).